

I CLAIM:

1. An integrated circuit carrier which includes  
a wafer having at least one receiving zone, said at least one receiving zone being demarcated by a bore in the wafer;
- 5        a plurality of island-defining portions arranged about said at least one receiving zone, at least one island-defining portion having an electrical terminal electrically connected to an electrical contact of said at least one receiving zone; and  
              a rigidity-reducing arrangement connecting each island-defining portion to each of its neighboring island-defining portions.
- 10      2. The carrier of claim 1 in which the bore is a recess defined in the wafer.
3.      The carrier of claim 1 in which the bore is a passage extending through the wafer from one surface of the wafer to an opposed surface of the wafer, the electrical contacts being arranged on the wafer about the passage.
- 15      4. The carrier of claim 3 which includes a mounting means for mounting the integrated circuit in its associated passage.
5.      The carrier of claim 1 in which the island-defining portions and the rigidity-reducing arrangements are formed by etching the wafer.
6.      The carrier of claim 5 in which said bore is also etched in the wafer.
7.      The carrier of claim 5 in which the etch is a re-entrant etch.
- 20      8. The carrier of claim 1 in which each rigidity-reducing arrangement is in the form of a serpentine member.
9.      The carrier of claim 1 in which each of those island-defining portions bordering their associated receiving zones is connected to said receiving zone by a secondary rigidity-reducing arrangement.
- 25      10. The carrier of claim 9 in which the secondary rigidity-reducing arrangement comprises a zig-zag element.
11.     The carrier of claim 1 in which the electrical terminal of each island-defining portion is in the form of a metal pad.
- 30      12. The carrier of claim 1 in which the wafer is of the same material as the integrated circuit to have a co-efficient of thermal expansion approximating that of the integrated circuit.